

# LH534R00A

CMOS 4M (512K × 8) Mask-Programmable ROM

## FEATURES

- 524,288 words × 8 bit organization
- Access time: 120 ns (MAX.)
- Power consumption:
  - Operating: 357.5 mW (MAX.)
  - Standby: 550 μW (MAX.)
- Mask-programmable control pin:
  - Pin 1 –  $OE_1/\overline{OE}_1/DC$
  - Pin 24 –  $OE/\overline{OE}$
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  - 32-pin, 600-mil DIP
  - 32-pin, 525-mil SOP
  - 32-pin, 400-mil TSOP (Type II)

## DESCRIPTION

The LH534R00A is a 4M-bit mask-programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

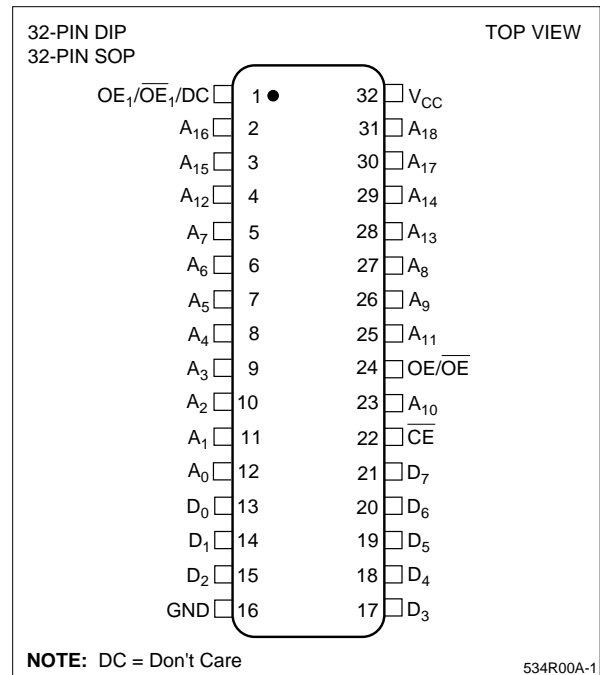


Figure 1. Pin Connections for DIP and SOP Packages

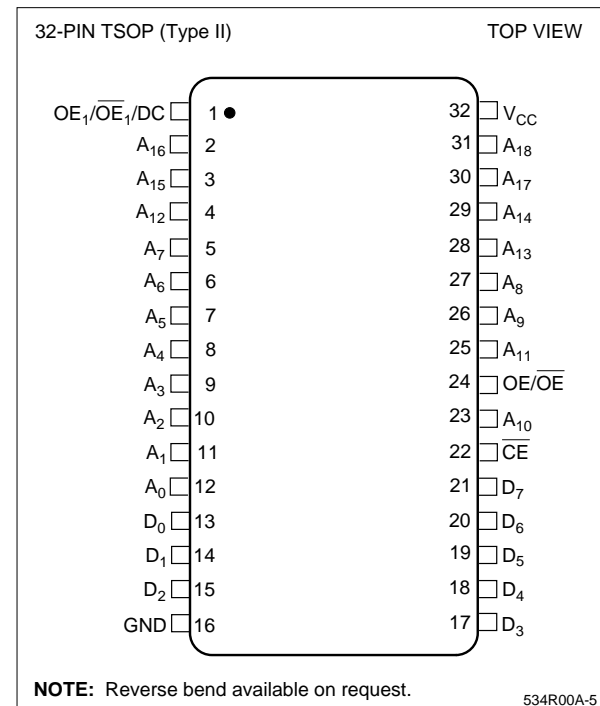


Figure 2. Pin Connections for TSOP Package

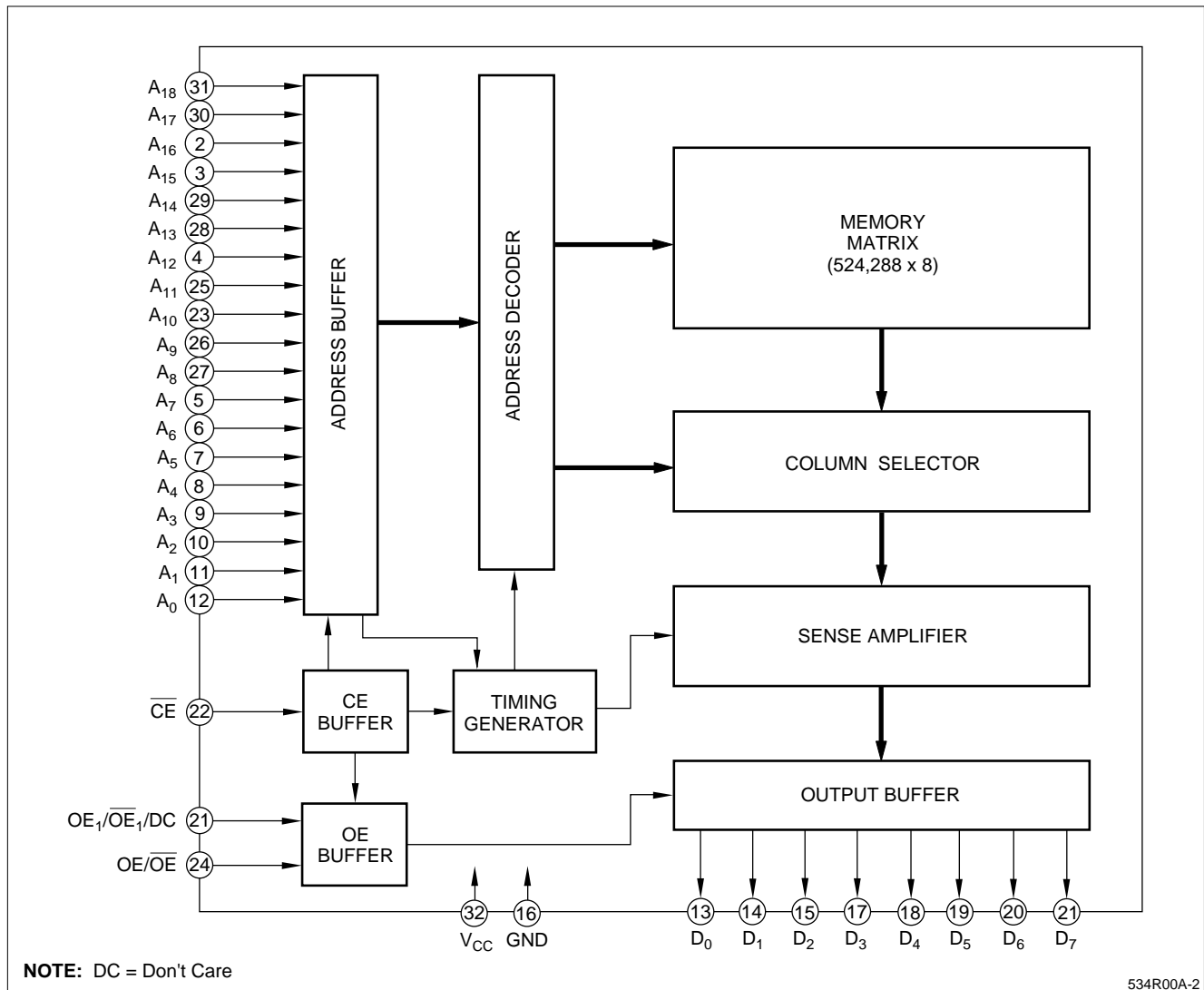


Figure 3. LH534R00A Block Diagram

## PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A <sub>0</sub> – A <sub>18</sub>	Address input	
D <sub>0</sub> – D <sub>7</sub>	Data output	
$\overline{CE}$	Chip Enable input	
OE/ $\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
OE <sub>1</sub> / $\overline{OE}$ <sub>1</sub> /DC	Output Enable input	1, 2
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

**NOTE:**

- Active levels of OE<sub>1</sub>/ $\overline{OE}$ <sub>1</sub>/DC and OE/ $\overline{OE}$  are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.
- DC = Don't care.

## TRUTH TABLE

$\overline{CE}$	$OE_1/\overline{OE}_1$	$OE/\overline{OE}$	D <sub>0</sub> – D <sub>7</sub>	SUPPLY CURRENT
H	X	X	High-Z	Standby (I <sub>SB</sub> )
L	L/H	X	High-Z	Operating (I <sub>CC</sub> )
L	X	L/H	High-Z	
L	H/L	H/L	Output	

## NOTE:

X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V <sub>CC</sub>	–0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V

DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ±10%, T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V <sub>IL</sub>		–0.3		0.8	V	
Input 'High' voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> + 0.3	V	
Output 'Low' voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA			0.4	V	
Output 'High' voltage	V <sub>OH</sub>	I <sub>OH</sub> = –400 μA	2.4			V	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>			10	μA	
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>			10	μA	1
Operating current	I <sub>CC1</sub>	t <sub>RC</sub> = 120 ns			65	mA	2
	I <sub>CC2</sub>	t <sub>RC</sub> = 1 μs			50		
	I <sub>CC3</sub>	t <sub>RC</sub> = 120 ns			60	mA	3
	I <sub>CC4</sub>	t <sub>RC</sub> = 1 μs			45		
Standby current	I <sub>SB1</sub>	$\overline{CE} = V_{IH}$			3	mA	
	I <sub>SB2</sub>	$\overline{CE} = V_{CC} - 0.2 V$			100	μA	
Input capacitance	C <sub>IN</sub>	f = 1 MHz			10	pF	
Output capacitance	C <sub>OUT</sub>	T <sub>A</sub> = 25°C			10	pF	

## NOTES:

- $\overline{CE}/OE/\overline{OE}_1 = V_{IH}$ ,  $OE/OE_1 = V_{IL}$
- V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>,  $\overline{CE} = V_{IL}$ , outputs open
- V<sub>IN</sub> = (V<sub>CC</sub> – 0.2 V) or 0.2 V,  $\overline{CE} = 0.2 V$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to }+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	120		ns	
Address access time	$t_{AA}$		120	ns	
Chip enable access time	$t_{ACE}$		120	ns	
Output enable delay time	$t_{OE}$		60	ns	
Output hold time	$t_{OH}$	0		ns	
CE to output in High-Z	$t_{CHZ}$		60	ns	1
OE to output in High-Z	$t_{OHZ}$		60	ns	

**NOTE:**

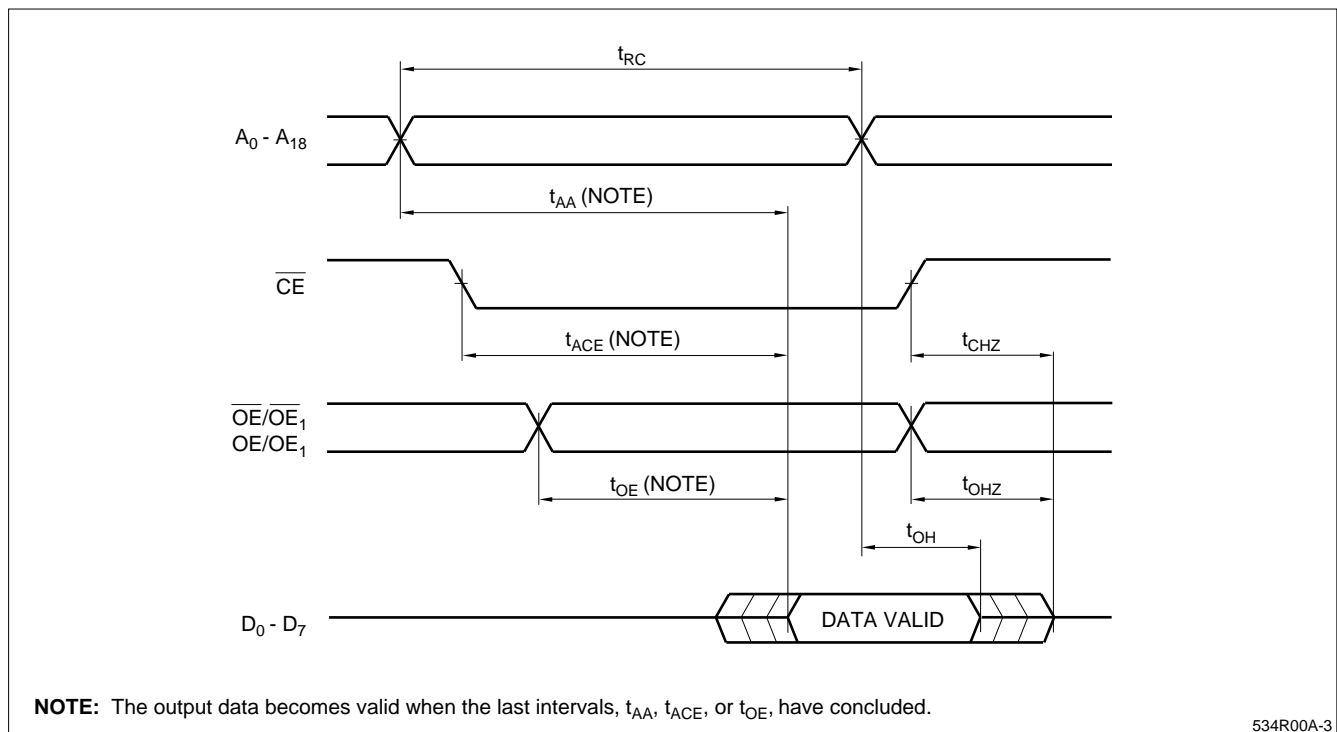
1. This is the time required for the outputs to become high-impedance.

**AC TEST CONDITIONS**

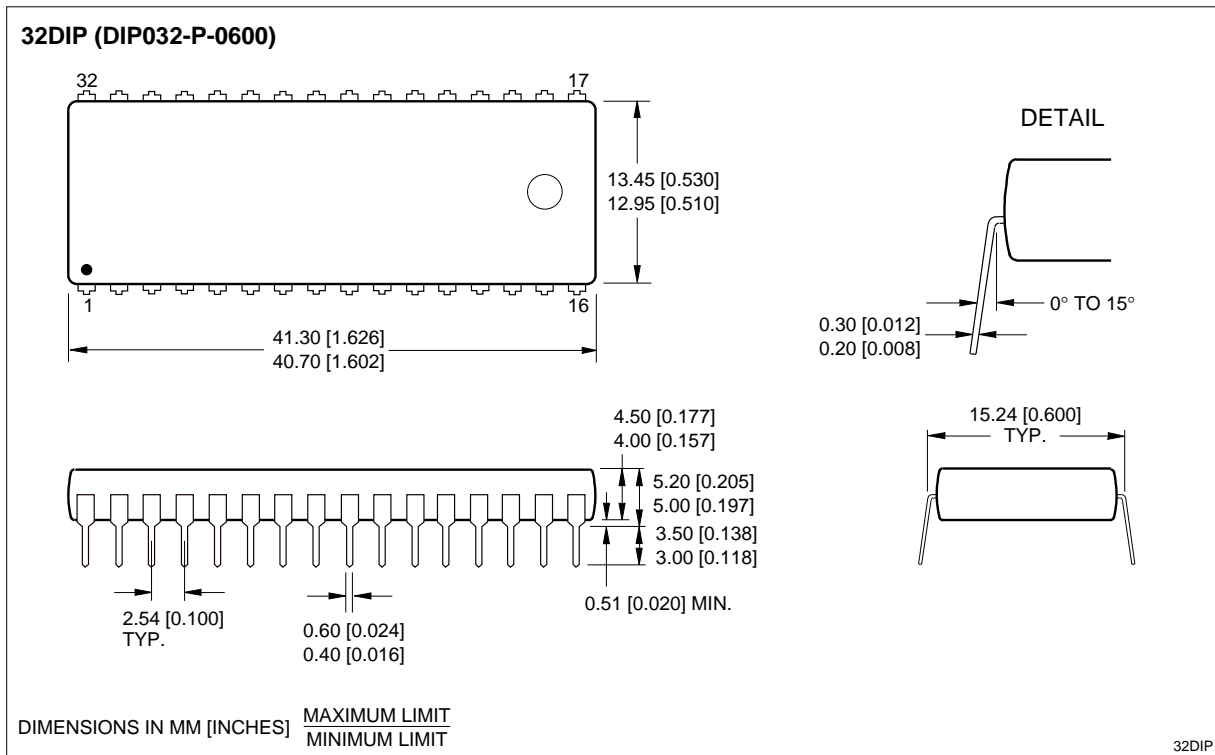
PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

**CAUTION**

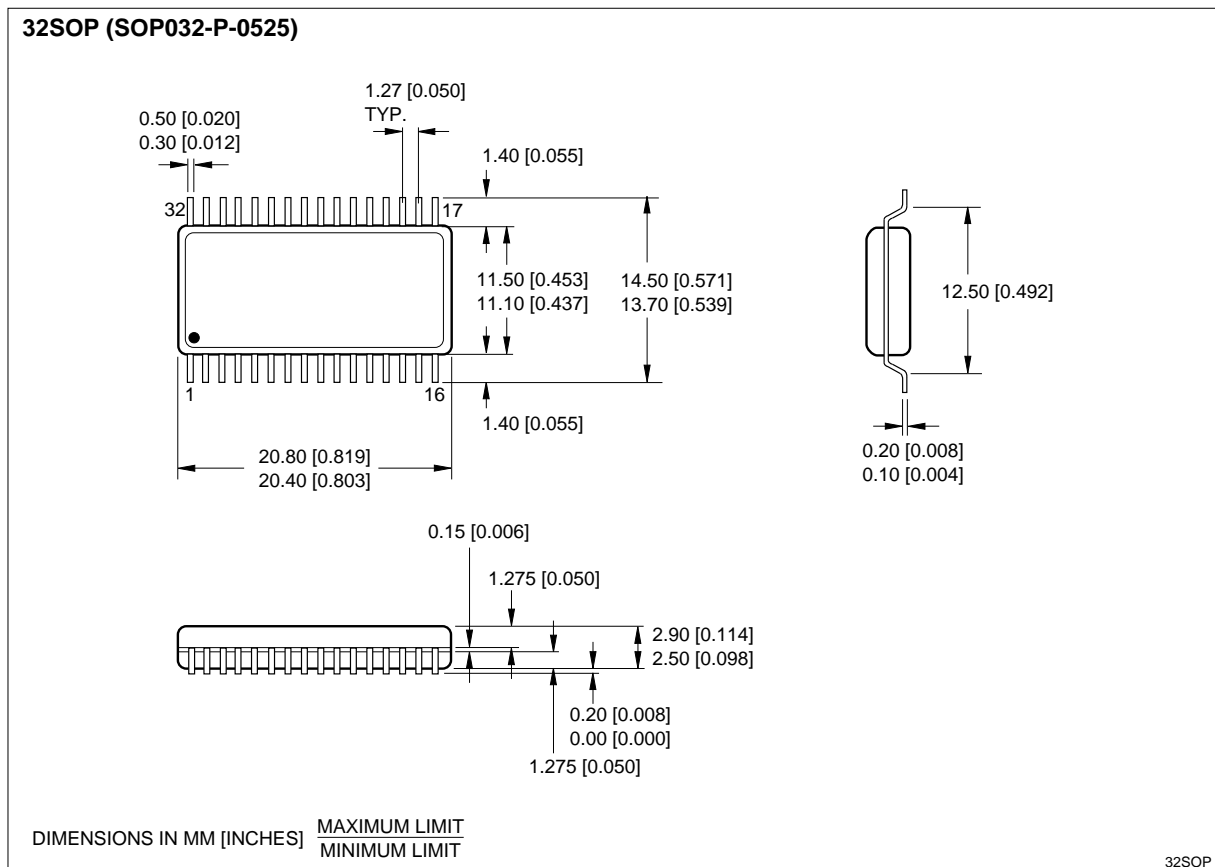
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.

**Figure 4. Timing Diagram**

PACKAGE DIAGRAMS



32-pin, 600-mil DIP



32-pin, 525-mil SOP

